CY28405

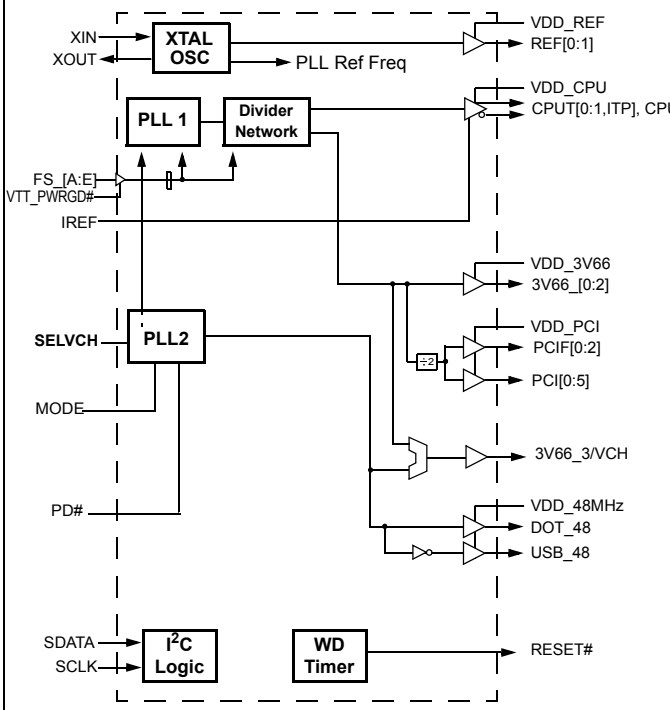
CK409-Compliant Clock Synthesizer

Features

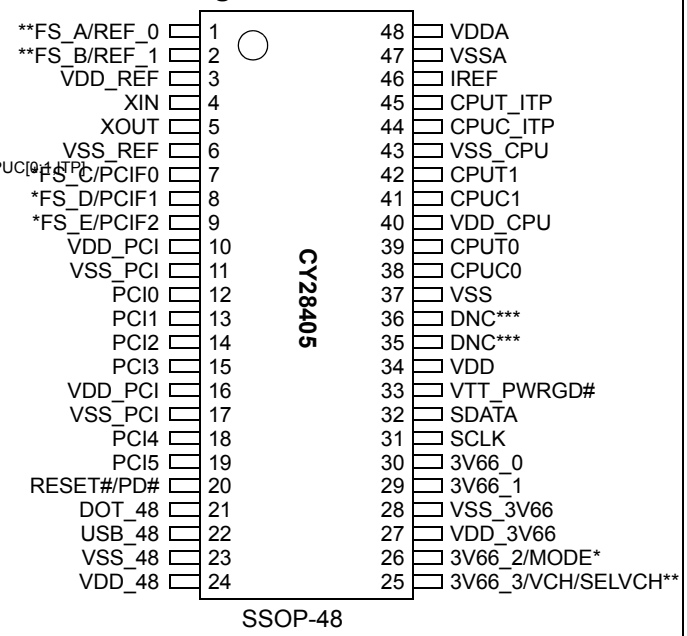
- **Supports Intel® Springdale/Prescott (CK409)**
- **Selectable CPU frequencies**
- **3.3V power supply**
- **Nine copies of PCI clock**
- **Four copies 3V66 clock with one optional VCH**
- **Two copies 48-MHz USB clock**
- **Two copies REF clock**
- **Three differential CPU clock pairs**
- **Dial-A-Frequency®**
- **Supports SMBus/I²C Byte, Word, and Block Read/Write**
- **Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction**
- **48-pin SSOP package**

CPU	3V66	PCI	REF	48M
x 3	x 4	x 9	x 2	x 2

Block Diagram



Pin Configuration



SSOP-48

* 150k Internal Pull-up
** 150k Internal Pull-down
*** Do Not Connect

Pin Description

Pin No.	Name	Type	Description
1, 2	REF(0:1)	O, SE	**Reference Clock**. 3.3V 14.318-MHz clock output.
1, 2, 7, 8, 9	FS_A, FS_B, FS_C, FS_D, FS_E	I	**3.3V LVTTL latched input for CPU frequency selection**.
4	XIN	I	**Crystal Connection or External Reference Frequency Input**. This pin has dual functions. It can be used as an external 14.318-MHz crystal connection or as an external reference frequency input.
5	XOUT	O, SE	**Crystal Connection**. Connection for an external 14.318-MHz crystal output.
39, 42, 45	CPUT(0:1,ITP)	O, DIF	**CPU Clock Output.** Differential CPU clock outputs.
38, 41, 44	CPUC(0:1,ITP)	O, DIF	**CPU Clock Output.** Differential CPU clock outputs.
36, 35	DNC		**Do Not Connect.**
30, 29	3V66(0:1)	O, SE	**66-MHz Clock Output.** 3.3V 66-MHz clock from internal VCO.
25	3V66_3/VCH/SELVCH	I/O, SE PD	**48- or 66-MHz Clock Output**. 3.3V selectable through external SELVCH strapping resistor and SMBus to be 66-MHz or 48-MHz. Default is 66-MHz. 0 = 66 MHz, 1 = 48 MHz
26	3V66_2/MODE	I/O, SE PU	**66-MHz Clock Output**. 3.3V 66-MHz clock from internal VCO. Reset or Power-down Mode Select. Selects between RESET# output or PWRDWN# input for the PWRDWN#/RESET# pin. Default is RESET#. 0 = PD#, 1 = RESET
7, 8, 9	PCIF(0:2)	O, SE	**Free Running PCI Output**. 33-MHz clocks divided down from 3V66.
12, 13, 14, 15, 18, 19	PCI(0:5)	O, SE	**PCI Clock Output**. 33-MHz clocks divided down from 3V66.
22	USB_48	O, SE	**Fixed 48-MHz clock output**.
21	DOT_48	O, SE	**Fixed 48-MHz clock output**.
46	IREF	I	**Current Reference**. A precision resistor is attached to this pin which is connected to the internal current reference.
20	RESET#/PD#	I/O, PU	**3.3V LVTTL input for Power-down# active LOW**. Watchdog Timeout Reset Output
33	VTT_PWRGD#	I	**3.3V LVTTL input is a level sensitive strobe used to latch the FS[A:E] input (active LOW)**.
32	SDATA	I/O	**SMBus compatible SDATA**.
31	SCLK	I	**SMBus compatible SCLOCK**.
48	VDDA	PWR	**3.3V Power supply for PLL**.
47	VSSA	GND	**Ground for PLL**.
3, 10, 16, 24, 27, 34, 40	VDD(REF,PCI,48,3V66,CPU,ITP)	PWR	**3.3V Power supply for outputs**.
6, 11, 17, 23, 28, 37, 43	VSS(REF,PCI,48,3V66, CPU,ITP)	GND	**Ground for outputs**.

MODE Select

The hardware strapping MODE input pin can be used to select the functionality of the RESET#/PD# pin. The default (internal pull up) configuration is for this pin to function as a RESET# Watchdog output. When pulled LOW during device power-up, the RESET#/PD# pin will be configured to function as a Power Down input pin.

Frequency Select Pins

Host clock frequency selection is achieved by applying the appropriate logic levels to FS_A through FS_E inputs prior to VTT_PWRGD# assertion (as seen by the clock synthesizer). Upon VTT_PWRGD# being sampled low by the clock chip (indicating processor VTT voltage is stable), the clock chip samples the FS_A through FS_E input values. For all logic levels of FS_A through FS_E, VTT_PWRGD# employs a one-shot functionality in that once a valid low on VTT_PWRGD# has been sampled, all further VTT_PWRGD# and FS_A through FS_E transitions will be ignored.

Table 1. Frequency Selection Table

Input Conditions					Output Frequency				
FS_E	FS_D	FS_C	FS_B	FS_A					
FSEL_4	FSEL_3	FSEL_2	FSEL_1	FSEL_0	CPU	3V66	PCI	VCO Freq.	PLL Gear Constants (G)
0	0	0	0	0	100.7	67.1	33.6	805.6	24004009.32
0	0	0	0	1	100.2	66.8	33.4	801.6	24004009.32
0	0	0	1	0	108.0	72.0	36.0	864.0	24004009.32
0	0	0	1	1	101.2	67.5	33.7	809.6	24004009.32
0	0	1	0	0	Reserved	Reserved	Reserved	Reserved	Reserved
0	0	1	0	1	Reserved	Reserved	Reserved	Reserved	Reserved
0	0	1	1	0	Reserved	Reserved	Reserved	Reserved	Reserved
0	0	1	1	1	Reserved	Reserved	Reserved	Reserved	Reserved
0	1	0	0	0	125.7	62.9	31.4	754.2	32005345.76
0	1	0	0	1	130.3	65.1	32.6	781.6	32005345.76
0	1	0	1	0	133.6	66.8	33.4	801.6	32005345.76
0	1	0	1	1	134.2	67.1	33.6	805.2	32005345.76
0	1	1	0	0	134.5	67.3	33.6	807.0	32005345.76
0	1	1	0	1	148.0	74.0	37.0	888.0	32005345.76
0	1	1	1	0	Reserved	Reserved	Reserved	Reserved	Reserved
0	1	1	1	1	Reserved	Reserved	Reserved	Reserved	Reserved
1	0	0	0	0	Reserved	Reserved	Reserved	Reserved	Reserved
1	0	0	0	1	Reserved	Reserved	Reserved	Reserved	Reserved
1	0	0	1	0	167.4	55.8	27.9	669.6	48008018.65
1	0	0	1	1	170.0	56.7	28.3	680.0	48008018.65
1	0	1	0	0	175.0	58.3	29.2	700.0	48008018.65
1	0	1	0	1	180.0	60.0	30.0	720.0	48008018.65
1	0	1	1	0	185.0	61.7	30.8	740.0	48008018.65
1	0	1	1	1	190.0	63.3	31.7	760.0	48008018.65
1	1	0	0	0	100.9	67.3	33.6	807.2	24004009.32
1	1	0	0	1	133.9	67.0	33.5	803.4	32005345.76
1	1	0	1	0	200.9	67.0	33.5	803.6	48008018.65
1	1	0	1	1	Reserved	Reserved	Reserved	Reserved	Reserved
1	1	1	0	0	100.0	66.7	33.3	800.0	24004009.32
1	1	1	0	1	133.3	66.7	33.3	800.0	32005345.76
1	1	1	1	0	200.0	66.7	33.3	800.0	48008018.65
1	1	1	1	1	Reserved	Reserved	Reserved	Reserved	Reserved

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initializes to their default setting upon power-up, and therefore use of this interface is optional. The interface can also be accessed during power-down operation.

Data Protocol

The clock driver serial protocol accepts Byte Write, Byte Read, Block Write and Block Read operation from any external I^2C controller. For Block Write/Read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For Byte Write and Byte Read operations, the system controller can access individual indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 2*.

The Block Write and Block Read protocol is outlined in *Table 3* while *Table 4* outlines the corresponding Byte Write and Byte Read protocol. The slave receiver address is 11010010 (D2h).

Table 2. Command Code Definition

Bit	Description
7	0 = Block Read or Block Write operation 1 = Byte Read or Byte Write operation
(6:0)	Byte offset for Byte Read or Byte Write operation. For Block Read or Block Write operations, these bits should be ‘0000000’

Table 3. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8-bit ‘00000000’ stands for block operation	11:18	Command Code – 8-bit ‘00000000’ stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29:36	Data byte 0 – 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 – 8 bits	30:37	Byte count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave – 8 bits
....	Data Byte N – 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave – 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave – 8 bits
		....	Not Acknowledge
		....	Stop

Table 4. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address – 7 bits	2:8	Slave address – 7 bits
9	Write = 0	9	Write = 0
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code – 8 bits '1xxxxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code – 8 bits '1xxxxxxx' stands for byte operation, bits[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte from master – 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address – 7 bits
29	Stop	28	Read = 1
		29	Acknowledge from slave
		30:37	Data byte from slave – 8 bits
		38	Not Acknowledge
		39	Stop

Byte 0: Control Register 0

Bit	@Pup	Name	Description
7	0		Reserved, Set= 0
6	1	PCIF PCI	PCI Drive Strength Override 0 = Force All PCI and PCIF Outputs to Low Drive Strength 1= Force All PCI and PCIF Outputs to High Drive Strength
5	0	Reserved	Reserved, Set= 0
4	HW	FS_E	Power up latched value of FS_E pin
3	HW	FS_D	Power up latched value of FS_D pin
2	HW	FS_C	Power up latched value of FS_C pin
1	HW	FS_B	Power up latched value of FS_B pin
0	HW	FS_A	Power up latched value of FS_A pin

Byte 1: Control Register 1

Bit	@Pup	Name	Description
7	0	Reserved	Reserved, set = 0
6	1	Reserved	Reserved, set = 1
5	1	Reserved	Reserved, set = 1
4	1	Reserved	Reserved, set = 1
3	1	Reserved	Reserved, set = 1
2	1	CPUT_ITP, CPUC_ITP	CPUT/C_ITP Output Enable 0 = Disabled (three-state), 1 = Enabled
1	1	CPUT1, CPUC1	CPU(T/C)1 Output Enable, 0 = Disabled (three-state), 1 = Enabled
0	1	CPUT0, CPUC0	CPU(T/C)0 Output Enable 0 = Disabled (three-state), 1 = Enabled

Byte 2: Control Register 2

Bit	@Pup	Name	Description
7	0	Reserved	Reserved, set = 0
6	0	Reserved	Reserved, set = 0
5	0	CPUT_ITP, CPUC_ITP	CPUT/C_ITP Pwrdwn drive mode 0 = Driven in power- down, 1 = three-state
4	0	CPUT1, CPUC1	CPU(T/C)1 Pwrdwn drive mode 0 = Driven in power-down, 1 = three-state
3	0	CPUT0, CPUC0	CPU(T/C)0 Pwrdwn drive mode 0 = Driven in power-down, 1 = three-state
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Byte 3: Control Register 3

Bit	@Pup	Name	Description
7	1		SW PCI_STP Function 0= PCI_STP assert, 1= PCI_STP deassert When this bit is set to 0, all STOPPABLE PCI and PCIF outputs will be stopped in a synchronous manner with no short pulses. When this bit is set to 1, all STOPPED PCI and PCIF outputs will resume in a synchronous manner with no short pulses.
6	1	Reserved	Reserved
5	1	PCI5	PCI5 Output Enable 0 = Disabled, 1 = Enabled
4	1	PCI4	PCI4 Output Enable 0 = Disabled, 1 = Enabled
3	1	PCI3	PCI3 Output Enable 0 = Disabled, 1 = Enabled
2	1	PCI2	PCI2 Output Enable 0 = Disabled, 1 = Enabled
1	1	PCI1	PCI1 Output Enable 0 = Disabled, 1 = Enabled
0	1	PCI0	PCI0 Output Enable 0 = Disabled, 1 = Enabled

Byte 4: Control Register 4

Bit	@Pup	Name	Description
7	0	USB_48	USB 48 Drive Strength Control 0 = High Drive Strength, 1 = Low Drive Strength
6	1	USB_48	USB_48 Output Enable 0 = Disabled, 1 = Enabled
5	0	PCIF2	Allow control of PCIF2 with assertion of SW PCI_STP 0 = Free Running, 1 = Stopped with SW PCI_STP
4	0	PCIF1	Allow control of PCIF1 with assertion of SW PCI_STP 0 = Free Running, 1 = Stopped with SW PCI_STP
3	0	PCIF0	Allow control of PCIF0 with assertion of SW PCI_STP 0 = Free Running, 1 = Stopped with SW PCI_STP
2	1	PCIF2	PCIF2 Output Enable 0 = Disabled, 1 = Enabled
1	1	PCIF1	PCIF1 Output Enable 0 = Disabled, 1 = Enabled
0	1	PCIF0	PCIF0 Output Enable 0 = Disabled, 1 = Enabled

Byte 5: Control Register 5

Bit	@Pup	Name	Description
7	1	DOT_48	DOT_48 Output Enable 0 = Disabled, 1 = Enabled
6	1	Reserved	Reserved
5	HW	3V66_3/VCH/SELVCH	3V66_3/VCH/SELVCH Frequency Select 0 = 3V66 mode, 1 = VCH (48MHz) mode May be written to override the power-up value.
4	1	3V66_3/VCH/SELVCH	3V66_3/VCH/SELVCH Output Enable 0 = Disabled,1 = Enabled
3	1	Reserved	Reserved
2	1	3V66_2	3V66_2 Output Enable 0 = Disabled, 1 = Enabled
1	1	3V66_1	3V66_1 Output Enable 0 = Disabled, 1 = Enabled
0	1	3V66_0	3V66_0 Output Enable 0 = Disabled, 1 = Enabled

Byte 6: Control Register 6

Bit	@Pup	Name	Description
7	0	REF PCIF PCI 3V66 3V66_3/VCH/SELVCH USB_48 DOT_48 CPUT, CPUT_ITP CPUC,CPUC_ITP	Test Clock Mode 0 = Disabled, 1 = Enabled When Test Clock Mode is enabled, the FS_A/REF_0 pin reverts to a dedicated FS_A input, allowing asynchronous selection between Hi-Z and REF/N mode.
6	0	Reserved	Reserved, Set = 0
5	0	Reserved	Reserved, Set = 0
4	0	Reserved	Reserved, Set = 0
3	0	Reserved	Reserved, Set = 0
2	0	PCIF PCI 3V66 CPUT,CPUT_ITP CPUC,CPUC_ITP	Spread Spectrum Enable 0 = Spread Off, 1 = Spread On
1	1	REF_1	REF_1 Output Enable 0 = Disabled, 1 = Enabled
0	1	REF_0	REF_0 Output Enable 0 = Disabled, 1 = Enabled

Byte 7: Vendor ID

Bit	@Pup	Name	Description
7	0		Revision Code Bit 3
6	1		Revision Code Bit 2
5	0		Revision Code Bit 1
4	0		Revision Code Bit 0
3	1		Vendor ID Bit 3
2	0		Vendor ID Bit 2
1	0		Vendor ID Bit 1
0	0		Vendor ID Bit 0

Byte 8: Control Register 8

Bit	@Pup	Name	Description
7	0	CPU PCIF PCI 3V66	Spread Spectrum Selection '000' = ±0.20% triangular '001' = + 0.12, – 0.62% '010' = + 0.25, – 0.75% '011' = –0.05, – 0.45% triangular '100' = ± 0.25% '101' = + 0.00, – 0.50% '110' = ± 0.5% '111' = ± 0.38%
6	1		
5	1		
4	0	FSEL_4	SW Frequency selection bits. See *Table 1*.
3	0	FSEL_3	
2	0	FSEL_2	
1	0	FSEL_1	
0	0	FSEL_0	

Byte 9: Control Register 9

Bit	@Pup	Name	Description
7	0	PCIF	PCIF Clock Output Drive Strength Control 0 = Low Drive strength, 1 = High Drive strength
6	0	PCI	PCI Clock Output Drive Strength 0 = Low Drive strength, 1 = High Drive strength
5	0	3V66	3V66 Clock Output Drive Strength 0 = Low Drive strength, 1 = High Drive strength
4	1	REF	REF Clock Output Drive Strength 0 = Low Drive strength, 1 = High Drive strength
3	1	Reserved	Reserved
2	1	Reserved	Reserved
1	0	Reserved	Vendor Test Mode (always program to 0)
0	0	Reserved	Vendor Test Mode (always program to 0)

Byte 10: Control Register 10

Bit	@Pup	Name	Description
7	0	PCI_Skew1	PCI skew control 00 = Normal 01 = –500 ps 10 = Reserved 11 = +500 ps
6	0	PCI_Skew0	
5	0	3V66_Skew1	3V66 skew control 00 = Normal 01 = –150 ps 10 = +150 ps 11 = +300 ps
4	0	3V66_Skew0	
3	1	Reserved	Reserved, Set = 1
2	1	Reserved	Reserved, Set = 1
1	1	Reserved	Reserved, Set = 1
0	1	Reserved	Reserved, Set = 1

Byte 11: Control Register 11

Bit	@Pup	Name	Description
7	0	Reserved	Vendor Test Mode (always program to 0)
6	0	Recovery_Frequency	This bit allows selection of the frequency setting that the clock will be restored to once the system is rebooted 0: Use Hardware settings 1: Use Last SW table Programmed values
5	0	Watchdog Time Stamp Reload	To enable this function the register bit must first be set to “0” before toggling to “1”. 0: Do not reload 1: Reset timer but continue to count.
4	0	WD_Alarm	This bit is set to “1” when the Watchdog times out. It is reset to “0” when the system clears the WD_TIMER time stamp
3	0	WD_TIMER3	Watchdog timer time stamp selection: 0000: Off 0001: 2 second 0010: 4 seconds 0011: 6 seconds . . . 1110: 28seconds 1111: 30seconds
2	0	WD_TIMER2	
1	0	WD_TIMER1	
0	0	WD_TIMER0	

Byte 12: Control Register 12

Bit	@Pup	Name	Description
7	0	CPU_FSEL_N8	If Prog_Freq_EN is set, the values programmed in CPU_FSEL_N[8:0] and CPU_FSEL_M[6:0] will be used to determine the CPU output frequency. The setting of FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[E:A] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used.
6	0	CPU_FSEL_N7	
5	0	CPU_FSEL_N6	
4	0	CPU_FSEL_N5	
3	0	CPU_FSEL_N4	
2	0	CPU_FSEL_N3	
1	0	CPU_FSEL_N2	
0	0	CPU_FSEL_N1	

Byte 13: Control Register 13

Bit	@Pup	Name	Description
7	0	CPU_FSEL_N0	If Prog_Freq_EN is set, the values programmed in CPU_FSEL_N[8:0] and CPU_FSEL_M[6:0] will be used to determine the CPU output frequency. The setting of FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[E:A] register will be used. When it is set, the frequency ratio stated in the SEL[4:0] register will be used.
6	0	CPU_FSEL_M6	
5	0	CPU_FSEL_M5	
4	0	CPU_FSEL_M4	
3	0	CPU_FSEL_M3	
2	0	CPU_FSEL_M2	
1	0	CPU_FSEL_M1	
0	0	CPU_FSEL_M0	

Byte 14: Control Register 14

Bit	@Pup	Name	Description
7	0	FS_(E:A)	FS_Override 0 = Select operating frequency by FS(E:A) input pins 1 = Select operating frequency by FSEL(4:0) settings
6	1	Reserved	Reserved, Set = 1
5	0	Reserved	Reserved, Set = 0

Byte 14: Control Register 14 (continued)

Bit	@Pup	Name	Description
4	0	Reserved	Reserved, Set = 0
3	0	Reserved	Reserved, Set = 0
2	0	Reserved	Reserved, Set = 0
1	0	Reserved	Reserved, Set = 0
0	0	Pro_Freq_EN	Programmable output frequencies enabled 0 = Disabled, 1 = Enabled

Dial-a-Frequency Programming

When the programmable output frequency feature is enabled (Pro_Freq_EN bit is set), the CPU output frequency is determined by the following equation:

Fcpu = G * N/M

“N” and “M” are the values programmed in Programmable Frequency Select N-Value Register and M-Value Register, respectively.

“G” stands for the PLL Gear Constant, which is determined by the programmed value of FS[E:A] or SEL[4:0]. The value is listed in *Table 1*.

The ratio of N and M need to be greater than “1” [N/M> 1].

The following table lists set of N and M values for different frequency output ranges. This example use a fixed value for the M-Value Register and select the CPU output frequency by changing the value of the N-Value Register.

Table 5. Examples of N and M Value for Different CPU Frequency Range

Frequency Ranges	Gear Constants	Fixed Value for M-Value Register	Range of N-Value Register for Different CPU Frequency
100 –125	24004009.32	48	200 – 250
126 – 166	32005345.76	48	189 – 249
167 – 200	48008018.65	48	167 – 200

Crystal Recommendations

The CY28405 requires a **Parallel Resonance Crystal**. Substituting a series resonance crystal will cause the CY28405 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It’s a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is **not true**.

Table 6. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	50 ppm	50 ppm	5 ppm

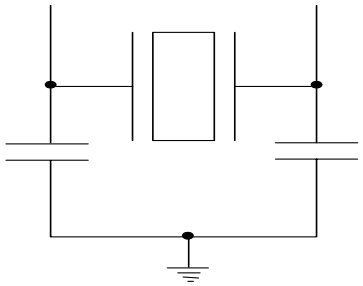


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.

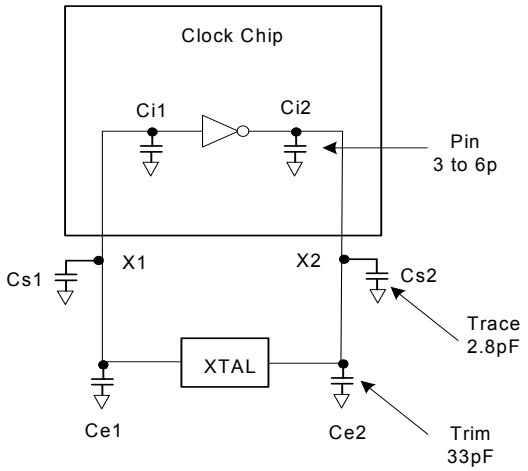


Figure 2. Crystal Loading Example

As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This mean the total capacitance on each side of the crystal must be twice the specified load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitative loading on both sides.

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL ..... Crystal load capacitance

CLe ..... Actual loading seen by crystal using standard value trim capacitors

Ce ..... External trim capacitors

Cs ..... Stray capacitance (trace,etc)

Ci ..... Internal capacitance (lead frame, bond wires etc)

PD# (Power-down) Clarification

The PD# pin is used to shut off all clocks and PLLs without having to remove power from the device. All clocks are shut down in a synchronous manner so has not to cause glitches while transitioning to the power down state.

PD# – Assertion

When PD# is sampled LOW by two consecutive rising edges of the CPUC clock then all clock outputs (except CPUT) clocks must be held LOW on their next HIGH to LOW transition. CPU clocks must be held with CPUT clock pin driven HIGH with a value of 2x Iref and CPUC undriven as the default condition. There exists an I^2C bit that allows for the CPUT/C outputs to be three-stated during power-down. Due to the state of internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete

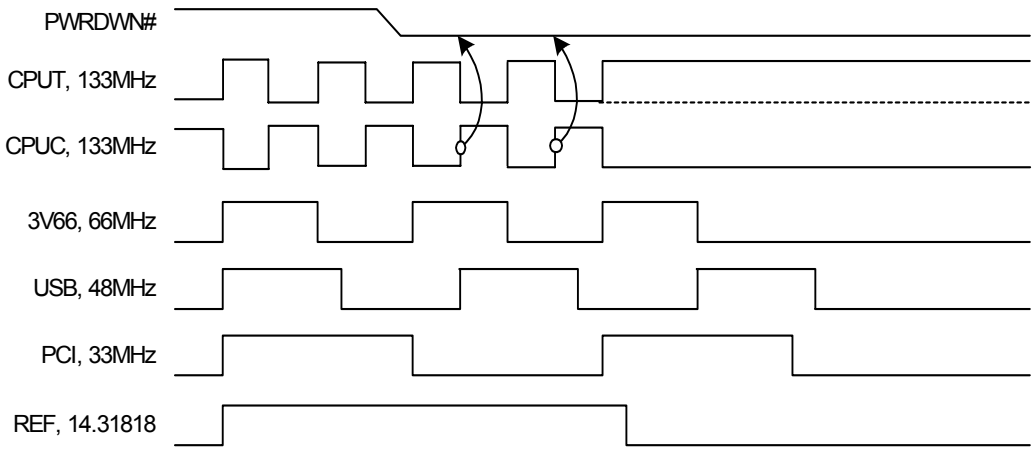


Figure 3. Power-down Assertion Timing Waveforms

PD# Deassertion

The power-up latency between PD# rising to a valid logic '1' level and the starting of all clocks is less than 1.8 ms. The CPUT/C outputs must be driven to greater than 200 mV is less than 300 μs.

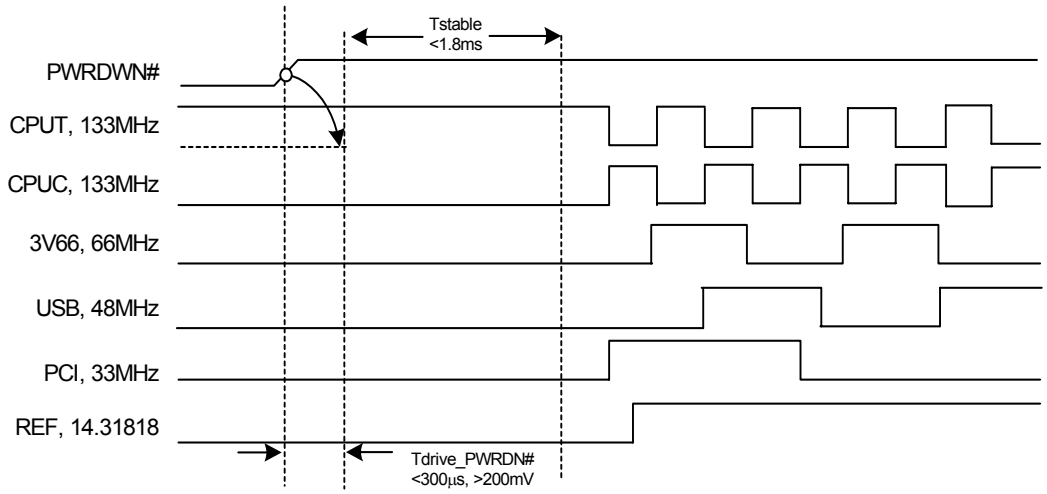


Figure 4. Power-down Deassertion Timing Waveforms

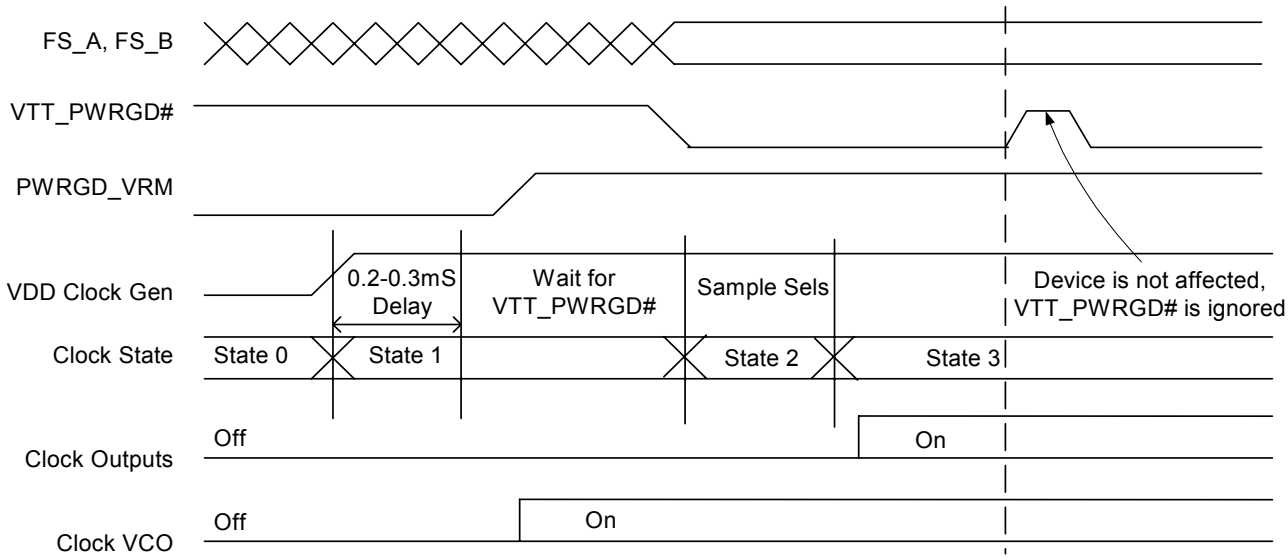


Figure 5. VTT_PWRGD Timing Diagram

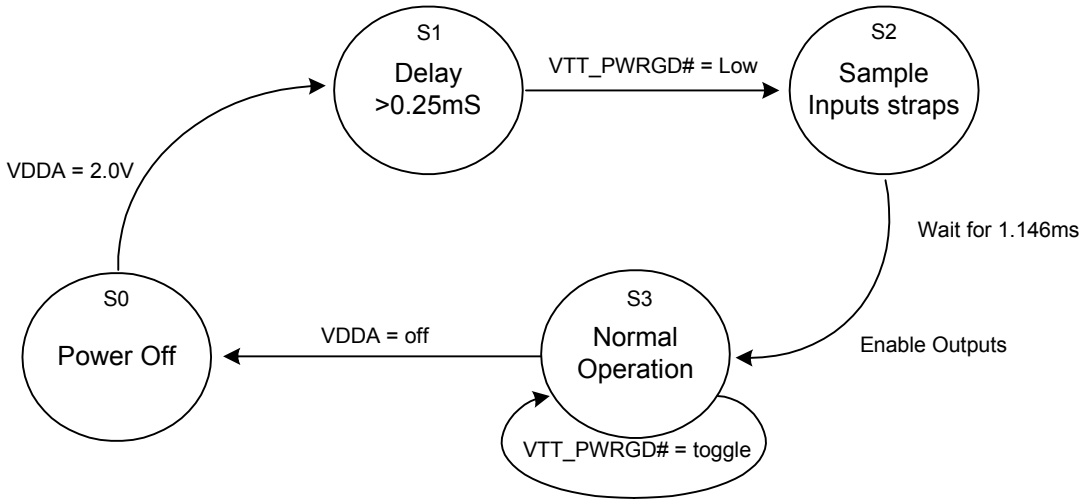


Figure 6. Clock Generator Power-up/Run State Diagram

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Core Supply Voltage		–0.5	4.6	V
V_{DDA}	Analog Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non-functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Functional	0	70	°C
T_J	Temperature, Junction	Functional	–	150	°C
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
$Ø_{JC}$	Dissipation, Junction to Case	Mil-Spec 883E Method 1012.1	15		°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	45		°C/W
UL–94	Flammability Rating	At 1/8 in.	V – 0		
MSL	Moisture Sensitivity Level		1		
Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.					

DC Electrical Specifications

Parameter	Description	Conditions	Min.	Max.	Unit
V_{DD}, V_{DDA}	3.3 Operating Voltage	3.3V ± 5%	3.135	3.465	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	–	1.0
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	–
V_{IL}	Input Low Voltage		V_{SS} – 0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{DD} + 0.5	V
I_{IL}	Input Leakage Current	Except Pull-ups or Pull-downs $0 < V_{IN} < V_{DD}$	–5	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 1 mA	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1 mA	2.4	–	V
I_{OZ}	High-impedance Output Current		–10	10	µA
C_{IN}	Input Pin Capacitance		2	5	pF
C_{OUT}	Output Pin Capacitance		3	6	pF
L_{IN}	Pin Inductance		–	7	nH
V_{XIH}	Xin High Voltage		$0.7V_{DD}$	V_{DD}	V
V_{XIL}	Xin Low Voltage		0	$0.3V_{DD}$	V
I_{DD}	Dynamic Supply Current	At 200 MHz and all outputs loaded per *Table 9* and *Figure 7*	–	280	mA
I_{PD}	Power-down Supply Current	PD# Asserted	–	1	mA

AC Electrical Specifications

Parameter	Description	Conditions	Min.	Max.	Unit
Crystal					
T_{DC}	XIN Duty Cycle	The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T_{PERIOD}	XIN period	When Xin is driven from an external clock source	69.841	71.0	ns
T_R / T_F	XIN Rise and Fall Times	Measured between $0.3V_{DD}$ and $0.7V_{DD}$	–	10.0	ns
T_{CCJ}	XIN Cycle to Cycle Jitter	As an average over 1 μs duration	–	500	ps
L_{ACC}	Long-term Accuracy	Over 150ms		300	ppm
CPU at 0.7V					
T_{DC}	CPUT and CPUC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	100-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	9.9970	10.003	ns
T_{PERIOD}	133-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	7.4978	7.5023	ns
T_{PERIOD}	200-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	4.9985	5.0015	ns
T_{SKEW}	Any CPU to CPU Clock Skew	Measured at crossing point V_{OX}	–	100	ps
T_{CCJ}	CPU Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	125	ps
T_R / T_F	CPUT and CPUC Rise and Fall Times	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	175	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/ (T_R + T_F)$	–	20	%
ΔT_R	Rise Time Variation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math average, see *Figure 7*	660	850	mv
V_{LOW}	Voltage Low	Math average,see *Figure 7*	–150	–	mv
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mv
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH}+0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 7*. Measure SE	–	0.2	V
3V66					
T_{DC}	3V66 Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Spread Disabled 3V66 Period	Measurement at 1.5V	14.9955	15.0045	ns
T_{PERIOD}	Spread Enabled 3V66 Period	Measurement at 1.5V	14.9955	15.0799	ns
T_{HIGH}	3V66 High Time	Measurement at 2.4V	4.9500	–	ns
T_{LOW}	3V66 Low Time	Measurement at 0.4V	4.5500	–	ns
T_R / T_F	3V66 Rise and Fall Times	Measured between 0.4V and 2.4V	0.5	2.0	ns
T_{SKEW}	Any 3V66 to Any 3V66 Clock Skew	Measurement at 1.5V	–	250	ps
T_{CCJ}	3V66 Cycle to Cycle Jitter	Measurement at 1.5V	–	250	ps
PCI/PCIF					
T_{DC}	PCIF and PCI Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.9910	30.0009	ns
T_{PERIOD}	Spread Enabled PCIF/PCI Period	Measurement at 1.5V	29.9910	30.1598	ns
T_{HIGH}	PCIF and PCI High Time	Measurement at 2.4V	12.0	–	ns

AC Electrical Specifications (continued)

Parameter	Description	Conditions	Min.	Max.	Unit
T_{LOW}	PCIF and PCI Low Time	Measurement at 0.4V	12.0	–	ns
T_R / T_F	PCIF and PCI Rise and Fall Times	Measured between 0.4V and 2.4V	0.5	2.0	ns
T_{SKEW}	Any PCI Clock to Any PCI Clock Skew	Measurement at 1.5V	–	500	ps
T_{CCJ}	PCIF and PCI Cycle to Cycle Jitter	Measurement at 1.5V	–	250	ps
DOT					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Period	Measurement at 1.5V	20.8257	20.8340	ns
T_{HIGH}	DOT High Time	Measurement at 2.4V	8.994	10.486	ns
T_{LOW}	DOT Low Time	Measurement at 0.4V	8.794	10.386	ns
T_R / T_F	Rise and Fall Times	Measured between 0.4V and 2.4V	0.5	1.0	ns
T_{CCJ}	Cycle to Cycle Jitter	10-µs period	–	350	ps
USB					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Period	Measurement at 1.5V	20.8257	20.8340	ns
T_{HIGH}	USB High Time	Measurement at 2.4V	8.094	10.036	ns
T_{LOW}	USB Low Time	Measurement at 0.4V	7.694	9.836	ns
T_R / T_F	Rise and Fall Times	Measured between 0.4V and 2.4V	1.0	2.0	ns
T_{CCJ}	Cycle to Cycle Jitter	125-µs period	–	350	ps
REF					
T_{DC}	REF Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	REF Period	Measurement at 1.5V	69.827	69.855	ns
T_R / T_F	REF Rise and Fall Times	Measured between 0.4V and 2.4V	1.0	4.0	V/ns
T_{CCJ}	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	1000	ps
ENABLE/DISABLE and SET-UP					
T_{STABLE}	All Clock Stabilization from Power-up		–	1.5	ms
T_{SS}	Stopclock Set-up Time		10.0	–	ns
T_{SH}	Stopclock Hold Time		0	–	ns

Table 7. Group Timing Relationship and Tolerances

Group	Conditions	Offset	
		Min.	Max.
3V66 to PCI	3V66 Leads PCI	1.5 ns	3.5 ns

Table 8. USB to DOT Phase Offset

Parameter	Typical	Value	Tolerance
DOT Skew	0°	0.0 ns	1000 ps
USB Skew	180°	0.0 ns	1000 ps
VCH SKew	0°	0.0 ns	1000 ps

Table 9. Maximum Lumped Capacitive Output Loads

Clock	Max Load	Units
PCI Clocks	30	pF
3V66 Clocks	30	pF
USB Clock	20	pF
DOT Clock	10	pF
REF Clock	30	pF

Test and Measurement Set-up

For Differential CPU and SRC Output Signals

The following diagram shows lumped test load configurations for the differential Host Clock Outputs.

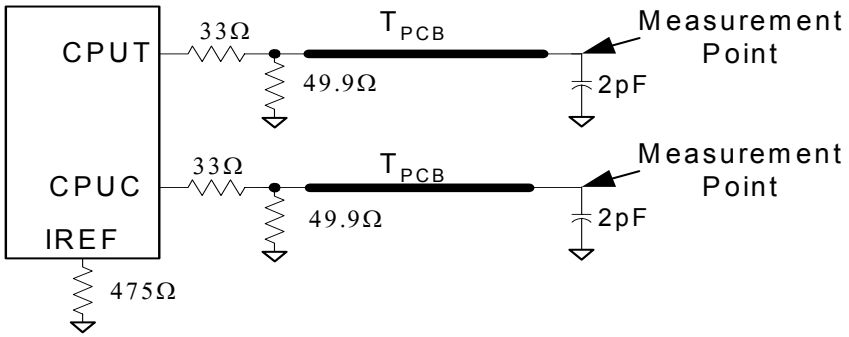


Figure 7. 0.7V Load Configuration

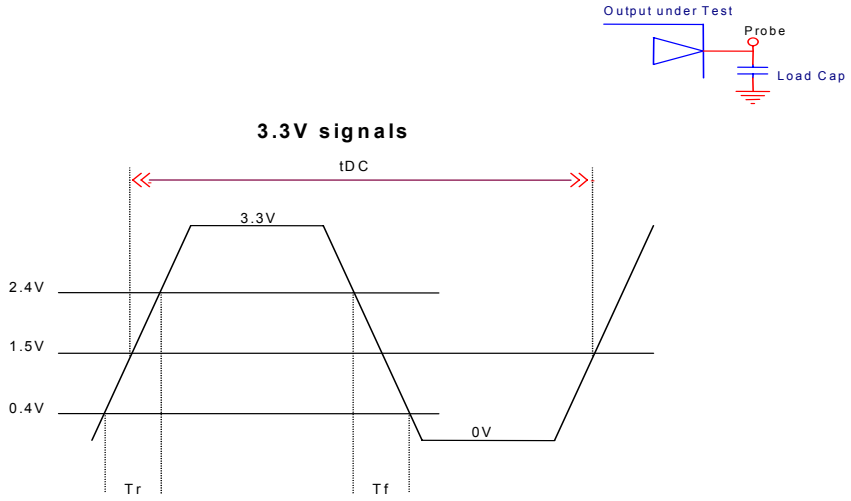


Figure 8. Lumped Load For Single-Ended Output Signals (for AC Parameter Measurement)

Table 10.CPU Clock Current Select Function

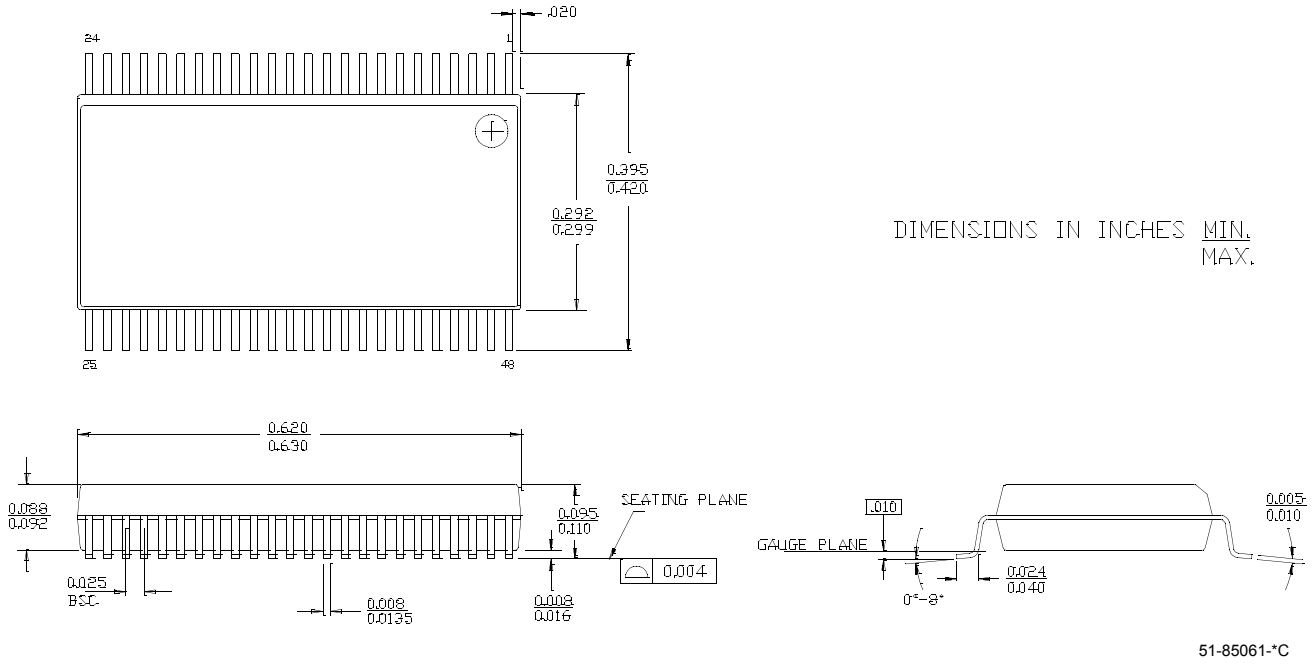
Board Target Trace/Term Z	Reference R, $I_{REF} – V_{DD} (3*R_{REF})$	Output Current	V_{OH} @ Z
50 Ohms	R_{REF} = 475 1%, I_{REF} = 2.32 mA	$I_{OH} = 6*I_{REF}$	0.7V @ 50

Ordering Information

Part Number	Package Type	Product Flow
CY28405OC	48-pin Shrunk Small Outline package (SSOP)	Commercial, 0° to 70°C
CY28405OCT	48-pin Shrunk Small Outline package (SSOP) – Tape and Reel	Commercial, 0° to 70°C
Lead Free		
CY28405OXC	48-pin Shrunk Small Outline package (SSOP)	Commercial, 0° to 70°C
CY28405OXCT	48-pin Shrunk Small Outline package (SSOP) – Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

48-Lead Shrunk Small Outline Package O48



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Document History Page

Document Title: CY28405 CK409-Compliant Clock Synthesizer Document Number: 38-07512				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	125354	04/15/03	RGL	New Data Sheet
*A	127159	06/16/03	RGL	Removed SRC functionality Modified the title to CK409-Compliant Clock Synthesizer
*B	235894	See ECN	RGL	Removed all items referencing to 166MHz Added Lead Free devices in the ordering information table